

PTO-1449 REPRODUCED  <b>SUPPLEMENTAL INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  November 19, 2004  (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.1003-013		APPLICATION NO. 10/691,111	
	FIRST NAMED INVENTOR Richard C. Foss		FILING DATE October 22, 2003	
	EXAMINER Hien N. Nguyen		CONFIRMATION NO. 5335	GROUP 2824

[illegible]

EXAMINER	H. NGUYEN	DATE CONSIDERED	2/11/05
----------	-----------	-----------------	---------



PTO-1449 REPRODUCED		ATTORNEY DOCKET NO. 2037.1003-013	APPLICATION NO. 10/691,111	
<b>SUPPLEMENTAL INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  November 19, 2004 (Use several sheets if necessary)		FIRST NAMED INVENTOR Richard C. Foss		FILING DATE October 22, 2003
		EXAMINER Hien N. Nguyen	CONFIRMATION NO. 5335	GROUP 2824

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

HN	AS	Sugibayashi, T., et al., "A 30ns 256Mb DRAM with Multi-Divided Array Structure," <i>IEEE International Solid-State Circuits Conference</i> , Session 3 (1993).
HN	AT	Sugibayashi, T., et al., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure," <i>IEEE Journal of Solid-State Circuits</i> , V. 28, No. 11 (1993).
HN	AU	Horiguchi, M., et al., "A Flexible Redundancy Technique for High-Density DRAM's," <i>IEEE Journal of Solid-State Circuits</i> , V. 26, No. 1 (1991).
HN	AV	Kimura, K., et al., "A Block-Oriented RAM with Half-Sized DRAM Cell and Quasi-Folded Data-Line Architecture," <i>IEEE Journal of Solid-State Circuits</i> , V. 26, No. 11 (1993).
HN	AW	Kimura, K., et al., "A Block-Oriented RAM with Half-Sized DRAM Cell and Quasi-Folded Data-Line Architecture," <i>IEEE International Solid-State Circuits Conference</i> , Session 6 (1991).
HN	AX	Dosaka, K., et al., "A 100MHz 4Mb Cache DRAM with Fast Copy-Back Scheme," <i>IEEE International Solid-State Circuits Conference</i> , Session 9 (1992).
HN	AY	Dosaka, K., et al., "A 100-MHz 4-Mb Cache DRAM with Fast Copy-Back Scheme," <i>IEEE Journal of Solid-State Circuits</i> , V. 27, No. 11 (1992).
HN	AZ	Kalter, H., et al., "A 50-ns 16-Mb DRAM with a 10-ns Data Rate and On-Chip ECC," <i>IEEE Journal of Solid-State Circuits</i> , V. 25, No. 5 (1990).

EXAMINER H. NGUYEN	DATE CONSIDERED 2/11/05
-----------------------	----------------------------